

**IN THE CLAIMS:**

Please CANCEL claim 19, without prejudice or disclaimer.

Please AMEND the claims in accordance with the following:

1. (CANCELED).
2. (PREVIOUSLY PRESENTED) The computer as claimed in claim 21, wherein said data holding part includes a plurality of registers.
3. (CURRENTLY AMENDED) The computer as claimed in claim 2, said computer further comprising flags each of said flags indicating whether said data is held in said ~~register~~plurality of registers.
4. (PREVIOUSLY PRESENTED) The computer as claimed in claim 21, said computer further comprising a data storing part, wherein said data holding part holds said data to be stored in said data storing part at a time when said interrupt occurs while a store instruction is executed, said store instruction requesting that said data is stored in said data storing part.
5. (PREVIOUSLY PRESENTED) The computer as claimed in claim 21, wherein said data holding part holds an instruction address of an instruction which causes said interrupt.
6. (CANCELED).
7. (PREVIOUSLY PRESENTED) The computer as claimed in claim 21, wherein said data holding part holds an effective address of a load instruction or a store instruction when said interrupt occurs while said load instruction or said store instruction is executed.
8. (PREVIOUSLY PRESENTED) The computer as claimed in claim 21, wherein said data is used for recovery from said interrupt.
9. (CANCELED).
10. (PREVIOUSLY PRESENTED) The control method as claimed in claim 22, wherein

said data is held in a plurality of registers and said data is used for recovery from a plurality of interrupts.

11. (CURRENTLY AMENDED) The control method as claimed in claim 10, wherein flags are used in which each of which flags indicates whether said data is held in said ~~register~~plurality of registers.

12. (CURRENTLY AMENDED) The control method as claimed in claim 22, said control method comprising ~~the step of~~:

holding said data to be stored in a data storing part in said computer at a time when said interrupt occurs while a store instruction is executed, said store instruction requesting that said data is stored in said data storing part.

13. (CURRENTLY AMENDED) The control method as claimed in claim 22, said control method comprising ~~the step of~~:

holding an instruction address of an instruction which causes said interrupt.

14. (CANCELED).

15. (CURRENTLY AMENDED) The control method as claimed in claim 22, said control method comprising ~~the step of~~:

holding an effective address of a load instruction or a store instruction when said interrupt occurs while said load instruction or said store instruction is executed.

16. (PREVIOUSLY PRESENTED) The control method as claimed in claim 22, wherein said data is used for recovery from said interrupt.

17. (CURRENTLY AMENDED) A computer processing method of plural instructions in parallel, and performing interrupt processing, comprising:

holding in a memory ~~at least an address~~ addresses of an instruction in an operation ~~the plural instructions~~ when the interrupt processing ~~that is not caused by the instruction causes the operation to halt~~ starts; and

~~continuing the operation after the interrupt processing is discontinued.~~

18. (CURRENTLY AMENDED) The computer processing method according to claim 17, ~~wherein said continuing of the operation includes~~further comprising continuing execution of the ~~instruction-instructions~~ based on the ~~address-addresses~~ held in the memory, ~~after the interrupt processing is discontinued.~~

19. (CANCELLED)

20. (PREVIOUSLY PRESENTED) The computer processing method according to claim 18, wherein the interrupt processing is initiated by an exception operation.

21. (CURRENTLY AMENDED) A computer which processes plural instructions in parallel, and which performs an interrupt process of a program caused by an exception operation when an interrupt occurs while an instruction in a program is executed, said computer comprising:

a data holding part holding data on all of instructions being executed of said instruction ~~that is interrupted by said interrupt~~ at a time when said interrupt starts to occur; and

~~at least one instruction execution part using the data held by said data holding part to continue execution of said instruction without rerunning said instruction.~~

22. (CURRENTLY AMENDED) A control method of a computer which processes plural instructions in parallel, and which performs an interrupt process of a program caused by an exception operation ~~when an interrupt occurs~~ while an instruction in a program is executed, said method comprising:

holding data on all of instructions being executed of said instruction ~~that is interrupted by said interrupt~~ at a time when said interrupt starts to occur; and

~~using the data held by said data holding part to continue execution of said instruction without rerunning said instruction.~~